Cadence Encounter Test User Guide

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Starting Encounter • To start the tool, first you must source the environment file source set_cadence_soc_env <CR> –This file sets up the paths and license file access to run First Encounter • Then on the command line type encounter <CR>

Cadence First Encounter Tutorial

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Encounter Conformal ECO Designer

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Advances in design methods and process technologies have resulted in a continuous increase in the complexity of integrated circuits (ICs). However, the increased complexity and nanometer-size features of modern ICs make them susceptible to manufacturing defects, as well as performance and quality issues. Testing for Small-Delay Defects in Nanoscale CMOS Integrated Circuits covers common problems in areas such as process variations, power supply noise, crosstalk, resistive opens/bridges, and design-for-manufacturing (DfM)-related rule violations. The book also addresses testing for small-delay defects (SDDs), which can cause immediate timing failures on both critical and non-critical paths in the circuit. Overviews semiconductor industry test challenges and the need for SDD testing, including basic concepts and introductory material Describes algorithmic solutions incorporated in commercial tools from Mentor Graphics Reviews SDD testing based on "alternative methods" that explores new metrics, top-off ATPG, and circuit topology-based solutions Highlights the advantages and disadvantages of a diverse set of metrics, and identifies scope for improvement Written from the triple viewpoint of university researchers, EDA tool developers, and chip designers and tool users, this book is the first of its kind to address all aspects of SDD testing from such a diverse perspective. The book is designed as a one-stop reference for current industrial practices, research challenges in the domain of SDD testing, and recent developments in SDD solutions.

This book will introduce new techniques for detecting and diagnosing small-delay defects in integrated circuits. Although this sort of timing defect is commonly found in integrated circuits manufactured with nanometer technology, this will be the first book to introduce effective and scalable methodologies for screening and diagnosing small-delay defects, including important parameters such as process variations, crosstalk, and power supply noise.

This book describes for readers a methodology for dynamic power estimation, using Transaction Level Modeling (TLM). The methodology exploits the existing tools for RTL simulation, design synthesis and SystemC prototyping to provide fast and accurate power estimation using Transaction Level Power Modeling (TLPM). Readers will benefit from this innovative way of evaluating power on a high level of abstraction, at an early stage of the product life cycle, decreasing the number of the expensive design iterations.

by Kurt Keutzer Those looking for a quick overview of the book should fast-forward to the Introduction in Chapter 1. What follows is a personal account of the creation of this book. The challenge from Earl Killian, formerly an architect of the MIPS processors and at that time Chief Architect at Tensilica, was to explain the significant performance gap between ASICs and custom circuits designed in the same process generation. The relevance of the challenge was amplified shortly thereafter by Andy Bechtolsheim, founder of Sun Microsystems and ubiquitous investor in the EDA industry. At a dinner talk at the 1999 International Symposium on Physical Design, Andy stated that the greatest near-term opportunity in CAD was to develop tools to bring the performance of ASIC circuits closer to that of custom designs. There seemed to be some synchronicity that two individuals so different in concern and character would be pre-occupied with the same problem. Intrigued by Earl and Andy’s comments, the game was afoot. Earl Killian and other veterans of microprocessor design were helpful with clues as to

the sources of the performance discrepancy: layout, circuit design, clocking methodology, and dynamic logic. I soon realized that I needed help in tracking down clues. Only at a wonderful institution like the University of California at Berkeley could I so easily commandeer an ab- bodied graduate student like David Chinnery with a knowledge of architecture, circuits, computer-aided design and algorithms.

Explains how to use low power design in an automated design flow, and examine the design time and performance trade-offs Includes the latest tools and techniques for low power design applied in an ASIC design flow Focuses on low power in an automated design methodology, a much neglected area

Sealed Lead Acid...Nickel Cadmium...Lithium Ion... How do you balance battery life with performance and cost? This book shows you how! Now that "mobile" has become the standard, the consumer not only expects mobility but demands power longevity in wireless devices. As more and more features, computing power, and memory are packed into mobile devices such as iPods, cell phones, and cameras, there is a large and growing gap between what devices can do and the amount of energy engineers can deliver. In fact, the main limiting factor in many portable designs is not hardware or software, but instead how much power can be delivered to the device. This book describes various design approaches to reduce the amount of power a circuit consumes and techniques to effectively manage the available power. Power Management Advice On: •Low Power Packaging Techniques •Power and Clock Gating •Energy Efficient Compilers •Various Display Technologies •Linear vs. Switched Regulators •Software Techniques and Intelligent Algorithms * Addresses power versus performance that each newly developed mobile device faces * Robust case studies drawn from the author's 30 plus years of extensive real world experience are included * Both hardware and software are discussed concerning their roles in power

The PMI-PBA® Exam Practice Test and Study Guide attempts to address all your questions and concerns by providing two of the most sought-after study aids: memory maps and practice questions. The systematic use of memory maps helps aid in the efficient recall of information and can boost confidence during the exam. Well-crafted practice questions are fantastic study aids that can be used to track your progress as you learn new concepts, introduce you to the complex sentence structure that is likely to appear on the exam, and concentrate your studies by domain, essentially preparing you to pass the very challenging PMI-PBA® Exam in the allotted four hours. In addition to study hints and exam topics, this book provides references to tools and techniques that should be incorporated into your work immediately. For each of the five domains outlined in the PMI Professional in Business Analysis (PMI-PBA)® Examination Content Outline 2013 (the ECO), twenty practice questions test your knowledge. Also included is a challenging 200-question practice exam, which is representative of the actual exam. To enhance your studies, a timed, online simulated exam is also provided. At the end of the simulated exam, you can see your score per the number of questions you answered correctly. These exam questions are crafted to foster learning and reinforce content; they are not obscure or overly complicated, but rather are representative of the actual exam. Knowing what to do must be translated into doing what you know. This book helps you prepare for the PMI-PBA® exam by instilling knowledge and encouraging critical thinking. As a result, the skills attained can lead to improved project success and outcomes, and you'll have a much stronger understanding of the material, along with the tools and techniques of business analysis. PMI-PBA® is a registered trademark of the Project Management Institute.

This book describes new and effective methodologies for modeling, analyzing and mitigating cell-

internal signal electromigration in nanoCMOS, with significant circuit lifetime improvements and no impact on performance, area and power. The authors are the first to analyze and propose a solution for the electromigration effects inside logic cells of a circuit. They show in this book that an interconnect inside a cell can fail reducing considerably the circuit lifetime and they demonstrate a methodology to optimize the lifetime of circuits, by placing the output, Vdd and Vss pin of the cells in the less critical regions, where the electromigration effects are reduced. Readers will be enabled to apply this methodology only for the critical cells in the circuit, avoiding impact in the circuit delay, area and performance, thus increasing the lifetime of the circuit without loss in other characteristics.